1. Introduction

$\text{Si}_{1-x}\text{Ge}_x$ ($x$: 0-1) thin films on insulators are expected as a material for next-generation thin film transistors and high-efficiency thin film solar cells [1]. Very recently, we have achieved a poly-Ge on an insulator with a hole mobility of 340 cm$^2$/Vs by using solid-phase crystallization (SPC). The key finding was the preparation of an amorphous Ge precursor whose atomic density was close to that of crystalline Ge by heating the substrate appropriately during the deposition. In this study, we apply this knowledge to $\text{Si}_{1-x}\text{Ge}_x$ and aim to improve the grain size and carrier mobility of SPC-$\text{Si}_{1-x}\text{Ge}_x$.

2. Experimental Procedures

Fig. 1 shows the sample preparation procedure. The amorphous $\text{Si}_{1-x}\text{Ge}_x$ thin films (100 nm thickness, $x = 0.5$, 0.75, and 1) were deposited on $\text{SiO}_2$ glass substrates using a molecular beam deposition system. The substrate temperature during the deposition $T_d$ was 50 and 125 °C. $T_d = 125$ °C is the optimum temperature for SPC-Ge. The samples were annealed at growth temperature $T_g$ = 550 °C for $x = 0.5$, 425 °C for $x = 0.75$, and 375 °C for $x = 1$ in a N$_2$ atmosphere to induce solid-phase crystallization.

3. Results and Discussion

Fig. 2 shows the EBSD images of the poly-$\text{Si}_{1-x}\text{Ge}_x$ layers. For the samples with $T_d = 50$ °C, Fig. 2 indicates that the grain size increases with decreasing $x$. This behavior is because of the fact that the margin of the activation energy between nucleation and growth increases with decreasing $x$. Fig. 2 also indicates that the grain size significantly increases by heating the substrate for Ge; however, this behavior is not so remarkable for SiGe. Fig. 3 shows the electrical properties of the poly-$\text{Si}_{1-x}\text{Ge}_x$ layers. The SPC-$\text{Si}_{1-x}\text{Ge}_x$ indicated p-type conduction. Because holes originate from point defects in Ge, the hole concentration decreases with decreasing Ge fraction, as shown in Fig. 3(a). Fig. 3(b) shows that the hole mobility is almost constant with Ge fraction for $T_d = 50$ °C. On the other hand, for $T_d = 125$ °C, the hole mobility increases with increasing Ge fraction. This behavior is attributed to the enlargement of the grain size which is dominant to Ge. The further optimization of $T_d$ for each Ge fraction will enable us to enhance the grain size and carrier mobility of the SPC-$\text{Si}_{1-x}\text{Ge}_x$ layers.