INFLUENCE OF THE THICKNESSES OF THE AMORPHOUS SILICON LAYERS ON THE EFFICIENCY OF SILICON HETEROJUNCTION SOLAR CELLS FOR VARIOUS CLIMATES

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Abstract
This work presents the influence of the intrinsic and doped amorphous silicon layers on the properties of a silicon heterojunction solar cell. Thickness series of all amorphous silicon layers were performed in both front and rear emitter to measure the impact of a given layer on the surface defect passivation, on the charge transport throughout the cell structure and on contact selectivity. Temperature dependent lifetime and IV measurements were performed to get an in depth understanding of the passivation mechanisms and of the effects of band offsets on charge extraction. Eventually, correlation between the different layers were evidenced. This study provides guidelines on the ideal structure for the fabrication of high-efficiency heterojunction solar cells, showing up to 22.7% efficiencies with devices employing standard PECVD amorphous silicon layers, industry-relevant ITO and screen printed silver as TCO and front metallization. It also gives insights on the best design to achieve a high energy yield for specific locations, exploiting the eventual improvements in efficiency for different irradiance and temperature when appropriate layer stacks are employed.

Experimental details
For this study, standard heterojunctions were fabricated using 240-µm-thick textured n-type float zone silicon wafers (2.8 Ωcm). Intrinsic and doped amorphous silicon layers were deposited by PECVD, then ITO and silver were sputtered to form 2x2 cm² cells where the front silver contacts were screen printed. The injection-dependent minority carrier lifetime was measured after PECVD, and temperature- and illumination-dependent IV and EQE measurements were performed on cells. Series resistance and ideality factor were also extracted to unravel their respective roles on the fill factor.

Preliminary results
As shown in figure 1, a strong trade-off is found between the surface passivation that requires a sufficient i-layer thickness and the series resistance that increases with i-layer thickness. This series resistance is due to energy barriers to charge transport, that can be overcome when using a higher temperature or a lower irradiance, making for a different optimum for maximal energy harvesting (depending on the location) compared to best efficiency under standard test conditions. The influence of the doped layers thickness will also be discussed as well as the interrelation between doped and intrinsic layers. For good transport, a thinner optimal layer thickness was observed for p-doped layers (~5 nm) than for n-doped layers (~20 nm), contrary to several reports, and can be related to the type of intrinsic layer used. Also, a degradation of lifetime upon deposition of the p-doped layer is seldom observed for thin intrinsic amorphous silicon layers, but it will be shown that with appropriate deposition conditions, this is not the case and an improvement of passivation can even be observed. The role of hydrogen will be discussed for both phenomenon. Based on this understanding, high-efficiency devices combining excellent passivation and transport properties could be made, and guidelines to tune such devices for different operating conditions (more relevant for field application) could be sketched.

Figure 1: Record IV curve at 25°C for standard a-Si layers

Figure 2: Effect of the intrinsic layer thickness on cell properties at variable temperatures