TOWARDS INDUSTRIALIZATION OF HETEROJUNCTION WITH THIN AND ULTRA-THIN WAFERS

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In a highly competitive PV market, reducing the production costs while maintaining high cell and module efficiencies is mandatory to remain attractive. In this context, reducing the silicon wafer thickness appears as a very promising approach as wafer production costs contribute for nearly 25% of the final price of the module. Furthermore, the mass-production availability of high-performance thin PV cells would be in-line with the growing demand for specific flexible or ultra-light module applications (space, aeronautics, BIPV...etc). Previous work [1] already demonstrated the industrial compatibility of thin wafers (240cm², 80-160µm thick range) with the heterojunction (SHJ) technology [2]. Cell integration was performed on CEA-INES Industrial LabFab pilot line [3]. High efficiencies, similar to the 160µm wafer thick references, were demonstrated for cells down to 90µm and first mini-modules with wafers down to 80µm were fabricated. Following these promising first results and learnings, we continuously ameliorated our production line to improve both thin cell efficiencies and breakage rate. In figure 1, typical impact of wafer thickness reduction on cell efficiency is presented for a four busbar (4BB) bifacial SHJ configuration. Compared to results presented in [1], efficiencies obtained have significantly been improved for all thicknesses considered. However, some efficiency loss is also now systematically observed when reducing the wafer thickness. Indeed, recent cell process improvements have translated in improved cell’s Voc output. The Jsc current losses related to the substrate thinning can thus no longer be compensated by a sufficient simultaneous Voc increase. Record cells obtained on such thin wafer remain nevertheless very promising, with 22.1% and 21.8% efficiency measured respectively on 115µm and 95µm 4BB SHJ bifacial devices. Breakage rate has also been greatly improved, with an overall non quality (TNQ) < 5% for production of 100µm thick wafers, but remains significantly higher in the 70-90µm range (TNQ >15%) where production automation adjustments are necessary. Nevertheless, ultimate wafer thicknesses batches (40-70µm) have been run to identify the actual limits of our production line. Despite critical breakage rate values (TNQ >30%) for such ultra-thin wafers, we were able to finalize and measure a significant amount of very thin wafer (60µm) and even bring some ultra-thin wafers (40µm) up to the final IV tester (efficiency >18.5% obtained on a 41µm thick 4BB bifacial SHJ cell). Finally, thanks to the previous mini-module learnings, two 60 cells modules have been fabricated, using standard glass, encapsulant and lamination process. A set of 93µm record SHJ cells has thus been integrated in a 60 cell glass/backsheet module configuration, leading to a very promising final module output power of 313Wc (CTM of 99.1%, no specific breakage observed after PL inspection) demonstrating the full compatibility of thin wafers with current module configuration.

Figure 1: Illustration of CEA recent achievements for SHJ cells and modules based on thin and ultra-thin wafers.